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10/629,112	07/29/2003	Junichi Sakamoto	450100-04668	6984

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William S. Frommer, Esq.
FROMMER LAWRENCE & HAUG LLP
745 Fifth Avenue
New York, NY 10151

EXAMINER	
WOODS, ERIC V	

ART UNIT	PAPER NUMBER
2672	

DATE MAILED: 12/16/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/629,112	SAKAMOTO ET AL.	
	Examiner	Art Unit	
	Eric V Woods	2672	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 July 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-12* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) _____ is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *29 July 2003* is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Priority

1. Receipt is acknowledged of papers submitted under 35 U.S.C. 119(a)-(d), which papers have been placed of record in the file.

Specification

2. The abstract of the disclosure is objected to because the first few lines do not clearly state what is being clipped – further, the wording is not proper idiomatic English. For example "able to increase the speed of the processing" – there should be a subject there (e.g. "processing of") or the terminology should be changed (e.g. with increased processing speed or "able to increase the processing speed."). Correction is required. See MPEP § 608.01(b).

3. The disclosure is objected to because of the following informalities: in numerous cases throughout the document, the letter 'e' is missing. For example, on page 1, line 24, the term "outsid" is used where the correct term would be "outside", the word judgment is misspelled without the vowel, etc.

4. The disclosure is objected because of the following informalities:

-On page 2, line 3, the phrase "according to if ..." is utilized, where this is clearly incorrect English and the phrase "according to" is unnecessary, redundant, and non-idiomatic English;

-Page 3, line 6, the word "judgments" is used as a verb, where the correct term would be "judges";

-Page 12, lines 9-10, the phrase "by for example" is used, which is not idiomatic English, where the correct phrase would be "for example".

Appropriate correction is required.

5. The disclosure is objected to because the "Brief Listing of Drawings" section does not include the different sub-drawings, e.g. it must list Figs. 12A-12G, 13A-13E, 14A-14D, 15A-15C, and16A-16B instead of merely reciting "Fig. 12".

6. The disclosure is objected to because the fourth coordinate of the system listed on page 10 is not defined – normally, when dealing with graphics a fourth coordinate represents alpha or an opacity value, but this is never specified.

7. The disclosure is objected to because a small, lower-case, superscripted letter 't' is present in the upper matrix operation illustrated on page 12. It is unclear what this letter is supposed to represent; examiner would presume that it represents taking the transpose of the inverse of the matrix M; if this is the case, the operation (taking the inverse) needs to be put in parentheses and the letter 't' needs to capitalized to properly illustrate the transpose operator and to illustrate order of precedence of the operators, e.g. it is otherwise unclear whether the inverse or the transpose is being taken first. Suggested formatting would be: $^{T}(M_u^{-1})$. This would be sufficiently clear.

8. The lengthy specification has not been checked to the extent necessary to determine the presence of all possible minor errors. Applicant's cooperation is requested in correcting any errors of which applicant may become aware in the specification.

Drawings

9. The drawings are objected to because in Figure 1, there is one bound (end of dashed line) that is denoted as 'W' that the specification on page 2 states is a bound that does not have a point on it – it is unclear that the location is the point indicated by the specification. This could be corrected by adding a point at the end of the dotted line there.

10. The drawings are objected to because in Figure 3, element 401 is labeled 'PRIM', wherein the specification labels it 'PROM'.

Corrected drawing sheets in compliance with 37 CFR 1.121(d) are required in reply to the Office action to avoid abandonment of the application. Any amended replacement-drawing sheet should include all of the figures appearing on the immediate prior version of the sheet, even if only one figure is being amended. The figure or figure number of an amended drawing should not be labeled as "amended." If a drawing figure is to be canceled, the appropriate figure must be removed from the replacement sheet, and where necessary, the remaining figures must be renumbered and appropriate changes made to the brief description of the several views of the drawings for consistency. Additional replacement sheets may be necessary to show the renumbering of the remaining figures. The replacement sheet(s) should be labeled "Replacement Sheet" in the page header (as per 37 CFR 1.84(c)) so as not to obstruct any portion of the drawing figures. If the changes are not accepted by the examiner, the applicant will be notified and informed of any required corrective action in the next Office action. The objection to the drawings will not be held in abeyance.

Claim Objections

11. Claims 1-12 are objected to because of the following informalities:

- The letter 'e' is missing from numerous words in all of the claims. This must be corrected. Appropriate correction is required.
- The term "vertexes" is used in all of the claims, where the correct, idiomatic English plural for the word "vertex" is "vertices", and "vertices" is most commonly used in computer graphics applications.

Appropriate correction is required.

Claim Rejections - 35 USC § 103

12. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> **(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.**

13. Claims 1-8 and 11-12 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koss et al (US 5,720,019)('Koss') in view of Inoue et al (US 5,982,380)('Inoue').

As to claim 1,

A clipping device for judging whether or not vertexes expressed by a predetermined coordinate system are inside or outside a multi-dimensional region of an object to be drawn, comprising (Koss Fig. 11, where a geometric primitive (triangle) is being tested over a bounding cube (13:59-67, 14:1-25), which is quintessentially the same operation as that shown in applicant's Figure 1, in which the geometric primitive under test is a point)(judging covered by judgment unit 20 of Inoue, Fig. 6):

-A clip code generation circuit for generating clip codes obtained by setting data in accordance with results of comparison of coordinates of said vertexes and a judgment reference value of said multi-dimensional region and a negative value of the judgment reference value as bit data; (See 11:60-67 and 12:1-10 where Koss discloses the generation of flags and clip sub-codes. Koss 2:45-55 discloses a clip code bus, which *prima facie* means that clip codes are being generated. Obviously, as shown above, comparisons are being made to check if primitives need to be clipped (13:59-67, 14:1-25), and coordinates are being compared and generating a trivial reject signal (3:12-35), where the vertices are tested as required (3:31-42). The trivial reject signal corresponds to the judgment signal recited by applicant. Vertex processing circuitry is disclosed (2:15-45) that actually performs the comparisons. Koss discloses (3:15-42) the half region and the clip region (3:1-4), which corresponds to the judgment reference value (and Fig. 11 as well) and the region in question. Since these comparisons are performed by digital computers, *prima facie* the data will be bit data, with further justification being that said clip codes would be transmitted utilizing the clip code bus. Further, such a 'trivial reject value' would of course have both positive and negative values, depending on the judgment when the vertex is checked for intersection with the clip region utilizing the vertex checking circuitry.)

-Clip registers for shifting the clip codes generated at said clip code generation circuit; and (Koss 9:38-51 discloses vertex clip code shift registers, which *prima facie* perform the recited functionality, since clip codes are *prima facie* generated by a clip code generating circuit and, if necessary, moved utilizing the clip code bus disclosed earlier.)

-A logic circuit for performing a logic operation with respect to all bit data set in said clip registers and setting a clip flag indicating whether or not a vertex to be judged is inside or outside the multi-dimensional region of the object to be drawn (A clip flag is taught in 11:60-67 and 12:1-10. Koss further discloses in 12:11-48, where flags are set if the region is entirely inside or outside of the clip region, which clearly utilizes shift registers, which are logic circuits (combinatorial logic is disclosed). This process of setting the flags is disclosed to happen once all the coordinates have been loaded (12:22-35).).
It would be obvious to modify the device of Koss, as described above, to have the components recited by applicant in whatever order required to meet the limitations of the claim. Reference Koss teaches all the limitations of the claim as discussed above in the specific points accompanying each part of the claim without explicitly having a so-called 'judgment signal' whereas the clipping circuit of Inoue explicitly provides the 'judgment signal' as noted above. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clipping circuit of Koss with the absolute values of Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Koss is meant to only accommodate standard (x, y, z) coordinates.

As to claim 2,

A clipping device as set forth in claim 1, wherein:

-Said coordinates of vertexes include values corresponding to a plurality of coordinate axes of the predetermined coordinate system, (Koss 1:23-45 discloses that computer graphics systems use x, y, z coordinate systems but more importantly, 2:21-51 clearly

discloses that the circuitry processes vertices that have x, y, z coordinates as applicant recites above)

-Said clip code generation circuit generates a plurality of clip codes corresponding to the coordinate axes, and (Koss 11:60-67 and 12:1-10 clearly illustrate that each coordinate (x, y, z) gets multiple clip codes as recited by applicant. See also Koss 12:24-34 for details on clip codes.)

-Said clip registers have a capacity for holding at least said plurality of clips codes. (Registers that hold clip codes are *prima facie* clip registers; Koss 9:38-51 clearly teaches vertex clip code shift registers. The clip code shift registers in question are taught in Koss 11:60-67, 12:1-10, and 12:24-34 to hold all the clip codes for the various coordinates after they have been processed, thus *prima facie* meeting the recited limitation of "holding at least said plurality of clip codes.")

Koss teaches all of the limitations of this claim as discussed above; since this rejection utilizes only the primary reference, no separate combination or motivation is required.

As to claim 3,

A clipping device as set forth in claim 1, wherein said clip code generation circuit generates said clip codes based on code data obtained by subtracting an absolute value of said judgment reference value from the absolute value of said vertex coordinates, code data of said vertex coordinates, and code data of said judgment reference value.

Reference Koss does not explicitly teach the use of an absolute value operator, but does teach the setting of a target volume with the area around it, and the checking of a vertex to see if it is in the test volume and within the clip volume and the setting of flags thereof. Reference Inoue teaches the use of absolute values in clipping preprocessing circuits, specifically 2:19-41 teaches that the clipping device performs an operation (subtraction) on the absolute value of a vertex coordinate and a pair of boundaries, wherein similar to Koss the clip data of the boundaries are put into the register and the check is performed, and the code data recited by applicant clearly is stored (from the axis basis). Further, Table 1 in Inoue illustrates (1:53-63) how codes are created for the view volume. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clipping circuit of Koss with the absolute values of Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Koss is meant to only accommodate standard (x, y, z) coordinates.

As to claim 4,

A clipping device as set forth in claim 2, wherein said clip code generation circuit said clip codes based on code data obtained by subtracting an absolute value of said judgment reference value from the absolute value of said vertex coordinates, code data of said vertex coordinates, and code data of said judgment reference value.

See the rejection to claim 3 above. The additional limitations of claim 2 are all taught by the primary reference as discussed in the rejection of claim 2. The claim wording is the same with the substitution of only "claim 2" for "claim 1". Therefore, the

entirety of that rejection, along with the motivation and combination, is incorporated herein by reference without further comment.

As to claim 5,

A clipping device for judging whether vertexes of a primitive expressed by a predetermined coordinate system are inside or outside of a multi-dimensional region of an object to be drawn, (Koss Fig. 11, where a geometric primitive (triangle) is being tested over a bounding cube (13:59-67, 14:1-25), which is quintessentially the same operation as that shown in applicant's Figure 1, in which the geometric primitive under test is a point) a polyhedron being drawn in units of primitives including a plurality of vertexes, (Inoue 2:2-11, where the polygons are decomposed into triangles, which clearly are primitives having a plurality of vertices, namely three) comprising:
-A clip code generation circuit for generating clip codes obtained by setting data in accordance with results of comparison of vertex coordinates of said primitives and a judgment reference value of said multi-dimensional region and a negative value of the judgment reference value as bit data for the amount of the vertexes of the primitive; (See 11:60-67 and 12:1-10 where Koss discloses the generation of flags and clip sub-codes. Koss 2:45-55 discloses a clip code bus, which *prima facie* means that clip codes are being generated. Obviously, as shown above, comparisons are being made to check if primitives need to be clipped (13:59-67, 14:1-25), and coordinates are being compared and generating a trivial reject signal (3:12-35), where the vertices are tested as required (3:31-42). The trivial reject signal corresponds to the judgment signal recited by applicant. Vertex processing circuitry is disclosed (2:15-45) that actually

performs the comparisons. Koss discloses (3:15-42) the half region and the clip region (3:1-4), which corresponds to the judgment reference value (and Fig. 11 as well) and the region in question. Since these comparisons are performed by digital computers, *prima facie* the data will be bit data, with further justification being that said clip codes would be transmitted utilizing the clip code bus. Further, such a 'trivial reject value' would of course have both positive and negative values, depending on the judgment when the vertex is checked for intersection with the clip region utilizing the vertex checking circuitry.)(Inoue teaches the same thing in 1:40-53, 2:21-40, and 3:31-40, wherein the clip codes are generated based on the comparison of the coordinates with the reference volume and the upper and lower values).

-A current clip register for a shifting the clip codes generated at said clip code generation circuit in accordance with a control signal; (Koss 9:38-51 discloses vertex clip code shift registers, which *prima facie* perform the recited functionality, since clip codes are *prima facie* generated by a clip code generating circuit and, if necessary, moved utilizing the clip code bus disclosed earlier. However, more specifically, Fig. 7 shows a shift register wherein coordinates are shifted in response to a control signal (12:30-60) and discloses how clip codes are shifted in that manner as well)(Inoue teaches registers for this processing in 2:19-41.)

-Clip registers of at least a number smaller than the number of vertexes of said primitive by one cascade connected to an output of said current clip register and able to replace the held data with the clip codes held by the register of a previous stage in accordance with a control signal; (Koss 9:38-51 discloses vertex clip code shift registers, which

prima facie perform the recited functionality (Fig. 7). Cascade connection is shown in Figure 4 with the elements shown being in horizontal configuration, which would back up the construction shown in Fig. 7, with the cascade construction stated in 9:51-57 because for six one bit cells to be connected together to create a six-bit register, they have to be cascaded. It would be obvious to use cascade connection even though the word "cascade" is not explicitly used; after all, this is the configuration shown in the drawings.)(Prima facie, shift instructions within the shift register that overwrite other coordinates or flags in that same register act as replacement operations.)

-A control circuit for outputting said control signal to the current clip register when receiving a clip code generation instruction to shift the clip codes generated at said clip code generation circuit and outputting said control signal to a corresponding clip register so as to replace the clip codes between adjacent clip registers including said current clip register when receiving a replacement instruction; (As discussed in the above paragraph, Koss 9:38-51 discusses the operation of such shift registers, which includes moving data as illustrated in Fig. 7 and structurally discussed in 9:51-58 (that is, that fulfills the adjacent shift register limitation (shown in Fig. 7) and the clip register limitation in general). The vertex load control line 224 for shift-registers (234, 236, 238, 240, 242, and 323, Koss Fig. 4) can be driven by the left stack control unit 122 – Koss Fig. 3) (10:1-24). Also, under some circumstances the shift registers can be controlled by the trivial accept and reject circuit shown below the shift registers in Fig. 4. Either the left stack control unit 122 or the accept/reject logic 250 in Fig. 4.)(Prima facie, shift instructions within the shift register that overwrite other coordinates or flags in that same

register act as replacement operations.)(Koss Figure 10 a flowchart of steps is shown. As the systems transitions from step 312 to 316 and complete processing a vertex, a flag is generated internally. Further, once step 316 is complete, the system generates results flag for all vertices (step 318). Koss further teaches in 6:31-47 that a replace mode can exist that will substitute one set of color values (object) for another (texture). Such a replace mode *prima facie* could obviously be applied to coordinates instead of colors (three values (x, y, z) (R, G, B)). Inoue 8:9-23 teaches that vertices are updated, that is, overwritten at a particular signal. Such replacement mode as discussed above would obviously be applied then, or if only one set of registers was being used, would be applied in between steps 312 and 316 in Koss if only one register were being used (and applicant's claim specifically states that it includes situations where only one register would be used).)

-A logic circuit for performing a logic operation with respect to all bits set in the clip registers including said current clip register and setting a clip flag indicating whether or not the vertex to be judged is inside or outside the multi-dimensional region of the object to be drawn (Koss clearly teaches this as the accept/reject logic element 250 in Fig. 4 (10:25-65).)

Reference Koss teaches all the limitations of the above claim except for explicitly stating certain details with regards to the clip code generating circuit [which Koss teaches implicitly, as explained in the detailed analysis and explanation following that particular limitation clause, as discussed above] that are taught by Inoue explicitly as mentioned above. It would have been obvious to one having ordinary skill in the art at

the time the invention was made to combine the clipping circuit of Koss with the absolute values of Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Koss is meant to only accommodate standard (x, y, z) coordinates but could be modified to handle more, but the configuration would be different.

As to claim 6,

A clipping device as set forth in claim 5, wherein said control circuit outputs said control signal to a corresponding clip register so as to replace the clip codes along with the vertex processing in accordance with the type of the primitive.

Reference Koss does not explicitly teach this limitation. Reference Inoue teaches in 1:40-67 and 2:1-11 that different amounts of memory (registers) are required for processing each kind of primitive. Koss teaches in 2:21-51 that the vertex processing circuitry can have three separate processing elements and that the circuitry has an enable input, which *prima facie* obviously could be modified such that each of the circuits had a separate enable function (which seems to borne out 10:20-25, where "enabled shift registers" are discussed, which proves that different registers can be disabled / enabled separately). Given that Koss has three units and Inoue teaches that each type of primitive would take one more set of shift registers (e.g. three primitive types – one, two, or three points or vertices requiring 6, 12, or 18 bits respectively), it would be obvious disable or enable registers based on the processing power required (e.g. the size of the primitive to be processed). The type of primitive would be selected during vertex processing and the appropriate shift registers would be enabled or

disabled by the control circuit (Koss 10:24-44) as required, which occurs during the initial vertex processing stage. Finally, Inoue has a dimension selection signal that would perform this function (11:25-32). It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clipping circuits of Koss and Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Koss is meant to only accommodate standard (x, y, z) coordinates but could be modified to handle more.

As to claim 7,

A clipping device as set forth in claim 5, wherein said control circuit generates a vertex ready flag indicating that the vertexes' worth of clip codes of said primitive are ready at the time of the replacement instruction.

Reference Koss does not explicitly teach this limitation, but in Figure 10 a flowchart of steps is shown. As the systems transitions from step 312 to 316 and complete processing a vertex, a flag is generated internally. Further, once step 316 is complete, the system generates results flag for all vertices (step 318). Koss further teaches in 6:31-47 that a replace mode can exist that will substitute one set of color values (object) for another (texture). Such a replace mode *prima facie* could obviously be applied to coordinates instead of colors (three values (x, y, z) (R, G, B)). Inoue 8:9-23 teaches that vertices are updated, that is, overwritten at a particular signal. Such replacement mode as discussed above would obviously be applied then, or if only one set of registers was being used, would be applied in between steps 312 and 316 in Koss if only one register were being used (and applicant's claim specifically states that it

includes situations where only one register would be used).) Further, a replacement mode could also be construed as occurring when the register values are shifted to generate the clip sub-does, as shown in Fig. 7 of Koss. It would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clipping circuits of Koss and Inoue, since Inoue is clearly designed to accommodate N dimensions (2:41-49) where Koss is meant to only accommodate standard (x, y, z) coordinates but could be modified to handle more.

As to claim 8,

A clipping device as set forth in claim 6, wherein said control circuit generates a vertex ready flag indicating that the vertexes' worth of clip codes of said primitive are ready at the time of execution of the replacement instruction.

See the rejection for claim 7, this claim is a substantial duplicate with only the words "claim 6" substituted for "claim 5."

As to claim 11,

A clipping device as set forth in claim 5, wherein:

-Said coordinates of said vertexes include values corresponding to a plurality of coordinate axes of a predetermined coordinate system,

-Said clip code generation circuit generates a plurality of clip codes corresponding to the coordinate axes, and

-Said clip registers have capacities for holding at least said plurality of clip codes.

See rejection to claim 2. Claim 11 is an exact duplicate of claim 2, and the only difference is the substitution of the words "claim 5" for "claim 1". The rejection is based only on the primary reference anyway.

As to claim 12,

A clipping device as set forth in claim 5,

-Wherein the clip code generation circuit generates said clip codes based on code data obtained by subtracting an absolute value of said judgment reference value from the absolute value of said vertex coordinates, code data of said vertex coordinates, and code data of said judgment reference values.

See rejection to claim 3. Claim 12 is an exact duplicate of claim 3, and the only difference is the substitution of the words "claim 5" for "claim 1". Therefore, the explanation, motivation, and combination are incorporated herein by reference without further comment.

14. Claims 9-10 are rejected under 35 U.S.C. 103(a) under Koss in view of Inoue as applied to claim 5 (and 6) above, and further in view of Oliver et al (US 5,313,610)('Oliver').

As to claim 9,

A clipping device as set forth in claim 5, wherein said control circuit selectively initializes a desired register among a plurality of clip registers including said current clip register under predetermined conditions.

References Koss and Inoue do not explicitly teach this limitation. Reference Oliver teaches (3:58-67) that registers are selected and initialized through a bus,

meaning that such registers can be individually selected and initialized. As shown in Oliver Fig. 2, the registers (40_1-40_K) are controlled by control logic 20 over said bus 14. It is well known in the art to initialize a register to prepare it for use in computational purposes or during a reset. Obviously, the control circuit of Oliver could perform the recited limitation of claim 9, since the clipping circuits of Koss and Inoue have multiple registers, including the "current clip register" recited by applicant as established in the rejections to earlier, parent claims. Given that shift operations where registers are overwritten are taught (e.g. Fig. 7 in Koss) and replace operations are taught (see discussion in the rejection for claim 7, also Inoue 8:9-23 teaches that vertices are updated, that is, overwritten at a particular signal), these would constitute circumstances that would generate "predetermined conditions" as recited by applicant. Given that Oliver teaches a control circuit for memory systems, e.g. register files, and Koss and Inoue have multiple registers that could *prima facie* obviously be embodied as a register file, it would have been obvious to one having ordinary skill in the art at the time the invention was made to combine the clip circuits of Koss and Inoue with the control logic of Oliver to achieve the selective initialization recited by applicant.

As to claim 10,

A clipping device as set forth in claim 6, wherein said control circuit selectively initializes a desired register among a plurality of clip registers including said current clip register under predetermined conditions.

See the rejection for claim 9; the claim is an exact duplicate of claim 9, with the exception that the words "claim 6" were substituted for "claim 5".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Eric V Woods whose telephone number is 703-305-0263. The examiner can normally be reached on M-F 7:30-5:00 alternate Fridays off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Michael Razavi can be reached on 703-305-4713. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Eric Woods

December 2, 2004

Jeffrey A. Brier
JEFFREY BRIER
PRIMARY EXAMINER